



The trainer provides all necessary inputs and connection for students to study decoding and demultiplexing of data transmitted by PCM transmitter. On-Board PLL provides regeneration of Clock. Synchronization between transmitter and receiver is provided by Pseudo random code.

Technical Specifications

Input Channel	: Time Division Multiplexed Serial Input
Demodulation	: Pulse code Demodulation
Clock Regeneration	: By phase Locked loop
Operating Speeds	: Fast - 320 KHz/Channel, Slow 1.9 Hz/Channel
Error Detection (Single bit)	: Off-Odd- Even parity & Hamming code
Error Correction	: Hamming code
PC- PC communication	: using 2 channels via RS232
Port	: 9 pin D type connector - 2 Nos.
Baud rate	: Selectable from 300 to 2400
Test Points	: 50
Interconnections	: 2 mm sockets
Power Supply	: 220 V \pm 10%, 50Hz / 60 Hz on request
Power Consumption	: 4 VA (approx.)

- Functional blocks indicated via on board mimics
- Input accepts two channel multiplexed data
- On board De-multiplexed PCM Receiver
- On board L. P. Filter
- Fast & Slow modes for real time operation and data flow examination
- On board PLL for clock regeneration
- On board sync code detector
- Error +check code options
- Odd or Even Parity-Single bit error detection
- Hamming code single bit error detection and correction
- 4 Switched faults allow different error check code option
- PC - PC Communication via RS232 interface

Experiments that can be performed

- PCM Demodulation Technique
- Time Division Demultiplexing of PCM data
- Clock Regeneration by PLL
- Effect of induced faults in the transmitter & receiver
- Signal recovery in 3 connecting modes between transmitter & receiver
- Clock & Frame Synchronization in PCM system
- PC -PC communication in 3 modes
- Study of synchronization by pseudo random code
- Study of error check codes
- Study of A/D conversion
- Study of control signals and their timing
- Study of time division multiplexing

Note: Specifications are subject to change.

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